Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of the Claims:

1. (Previously Presented) A semiconductor integrated circuit device comprising:

a plurality of static random access memory (SRAM) cells, each having a plurality of field effect transistors,

wherein each of said plurality of field effect transistors has a gate electrode thereof formed over a semiconductor substrate, a source region and a drain region formed in said semiconductor substrate, and a channel forming region formed in said semiconductor substrate and arranged between said source region and said drain region,

wherein a first field effect transistor selected from among said plurality of field effect transistors has a pair of semiconductor regions formed in said semiconductor substrate and serving as the source region and the drain region thereof such that end portions at a channel forming region side of said pair of semiconductor regions of said first field effect transistor are located in a direction away from opposite ends of the gate electrode of said first field effect transistor so as not be superposed with said gate electrode of said first field effect transistor, and

wherein said semiconductor integrated circuit device further comprises a second field effect transistor, which is formed on said semiconductor substrate and which is other than said first field effect transistor, said second field effect transistor having a pair of semiconductor regions formed in the semiconductor substrate and serving as the source region and the drain region thereof such that end portions at a channel forming region side

of said pair of semiconductor regions are partially superposed with the gate electrode of said second field effect transistor.

2. (Previously Presented) A semiconductor integrated circuit device according to claim 1, wherein a field effect transistor serving as a load of a SRAM cell is comprised of said first field effect transistor, and a field effect transistor for drive and selection of said SRAM cell is comprised of said second field effect transistor.

3. (Original) A semiconductor integrated circuit device according to claim 1, wherein said second field effect transistor comprises a field effect transistor of a peripheral circuit of the SRAM cells formed on said semiconductor substrate.

4. (Original) A semiconductor integrated circuit device according to claim 1, wherein said second field effect transistor comprises a field effect transistor of a logic circuit external to said SRAM cells.

5. (Original) A semiconductor integrated circuit device according to claim 1, wherein a plurality of said second field effect transistors comprise field effect transistors of a peripheral circuit of the SRAM cells and a logic circuit external to said SRAM cells.

6. (Previously Presented) A semiconductor integrated circuit device comprising:

at least a first field effect transistor and a second field effect transistor formed on a substrate, each of said first and second field effect transistors having a gate electrode formed over a principal surface of said substrate, and a source region and a drain region

formed at the principal surface of said substrate and separated by a channel forming region,

wherein each of the source and drain regions of said first field effect transistor has an end portion at the channel region side thereof located away from an end side of the gate electrode such that the source and drain region of the first field effect transistor are not superposed with the gate electrode thereof,

wherein each of the source and drain regions of said second field effect transistor has an end portion at the channel region side thereof which substantially coincides with an end side of the gate electrode or is superposed with a part of the gate electrode of the second field effect transistor, and

wherein said first and second field effect transistors are configured such that only said second field effect transistor contains a lightly doped drain (LDD) structure.

7. (Previously Presented) A semiconductor integrated circuit device according to claim 6, wherein said first field effect transistor is of a first channel conductivity type and said second field effect transistor is of a second, opposite channel conductivity type.

8. (Previously Presented) A semiconductor integrated circuit device according to claim 7, wherein each of said first and second field effect transistors is a metal insulator semiconductor field effect transistor (MISFET).

9. (Previously Presented) A semiconductor integrated circuit device according to claim 6, wherein said first and second field effect transistors have a same channel type conductivity.

10. (Previously Presented) A semiconductor integrated circuit device according to claim 9, wherein each of said first and second field effect transistors is a metal insulator semiconductor field effect transistor (MISFET).

11. (Previously Presented) A semiconductor integrated circuit device according to claim 8, wherein said first MISFET constitutes a MISFET in a static random access memory (SRAM) cell of a memory array and said second MISFET constitutes a MISFET in a peripheral circuit.

12. (Previously Presented) A semiconductor integrated circuit device according to claim 6, wherein said substrate is a semiconductor substrate in which the source and drain regions of each of said first and second field effect transistors are formed in a corresponding well region.

13. (Previously Presented) A semiconductor integrated circuit device according to claim 12, wherein each of said first and second field effect transistors is a metal insulator semiconductor field effect transistor (MISFET).

14. (Previously Presented) A semiconductor integrated circuit according to claim 8, wherein said first and second MISFETs are active elements in a static random access memory (SRAM) cell of a memory array.

15. (Previously Presented) A semiconductor integrated circuit device comprising:

a first field effect transistor and a second field effect transistor formed on a common semiconductor substrate, each of said first and second field effect transistors having an

insulated gate electrode formed on the substrate, and a source region and a drain region formed in the substrate and separated by a channel forming region,

wherein each of the source and drain regions of said first field effect transistor has an end portion at the channel region side thereof positionally offset away from an end side of the gate electrode such that the source and drain regions of the first field effect transistor are not superposed with the gate electrode thereof,

wherein at least one of the source and drain regions of said second field effect transistor has an end portion at the channel region side thereof which substantially coincides with an end side of the gate electrode or is overlapped, with respect to a plan view thereof, with a part of the gate electrode of said second field effect transistor, and

wherein only said second field effect transistor contains a lightly doped drain (LDD) structure.

16. (Previously Presented) A semiconductor integrated circuit device according to claim 15, wherein said first field effect transistor is of a first channel conductivity type and said second field effect transistor is of a second, opposite channel conductivity type.

17. (Previously Presented) A semiconductor integrated circuit device according to claim 16, wherein said first and second field effect transistors are active elements in a static random access memory (SRAM) cell of a memory array.

18. (Previously Presented) A semiconductor integrated circuit device according to claim 15, wherein said first and second field effect transistors have a same channel type conductivity.

19. (Previously Presented) A semiconductor integrated circuit device according to claim 15, wherein said first field effect transistor constitutes an active element in a memory array portion of the semiconductor substrate and said second field effect transistor constitutes an active element in a peripheral circuit portion of the semiconductor substrate.

20. (Previously Presented) A semiconductor integrated circuit device comprising:

a plurality of static random access memory (SRAM) cells, each having a pair of n-channel drive metal insulator semiconductor field effect transistors (MISFETs), a pair of p-channel load MISFETs and a pair of n-channel selection MISFETs,

wherein the n-channel drive MISFETs and n-channel selection MISFETs contain a lightly doped drain (LDD) structure, respectively, and

wherein the p-channel load MISFETs contain a single drain structure, respectively.

21. (Previously Presented) A semiconductor integrated circuit device according to claim 20, wherein each one of the n-channel drive MISFETs is coupled with one of the p-channel MISFETs to form an inverter circuit.

22. (New) A semiconductor integrated circuit device according to claim 20, wherein each of drain regions of the n-channel drive MISFETs and n-channel selection MISFETs is comprised of a first region and a second region, the first region has an impurity concentration of dopant greater than that of the second region, and each of the second regions of the n-channel drive MISFETs and n-channel selection MISFETs is disposed nearer to each of gate electrodes of the n-channel drive MISFETs and n-channels selection MISFETs than is the first region.